CCE4502 IO-Link Device IC with Integrated Frame Handler

1. Description

High-voltage interface ASSP with overvoltage, high current and high temperature protection, based on a 0.18 µm HV-CMOS technology. There is a wide range of supported applications with different packaging and configuration options. Typical applications are industrial sensors and actuators.

2. Features

- IO-Link Compliant Transceiver*
- Integrated UART (COM1-3)
- Hardware IO-Link Stack support
- All IO-Link M-sequence types supported
- One IO-Link slave channel with up to 200mA driving current
- Programmable PNP-, NPN- and Push-Pull mode
- Auxiliary multi-purpose 200mA Input-Output-Channel
- Slew rate control
- Reverse-polarity protection
- Low TC on-chip oscillator with ±2 % frequency accuracy
- Overcurrent protection
- Overvoltage and high temperature detection
- SPI interface
- Rich configuration options
- Evaluation board available
- QFN24 and CSP24 package

* IO-Link is a registered trademark of Profibus User Organization (PNO).

Contents

3. Block diagram

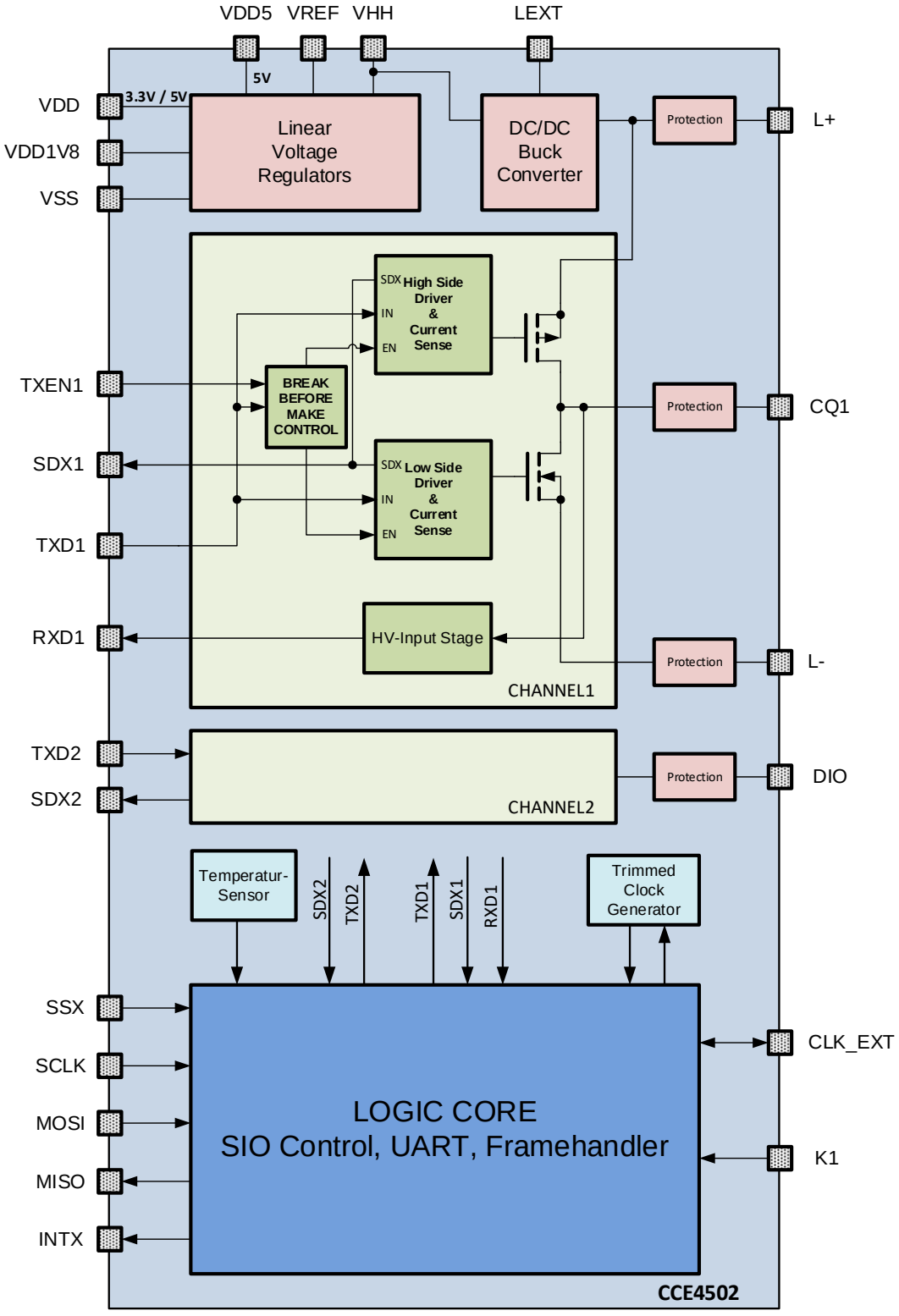


Figure 1: Block diagram

4. Pinout

4.1. Package

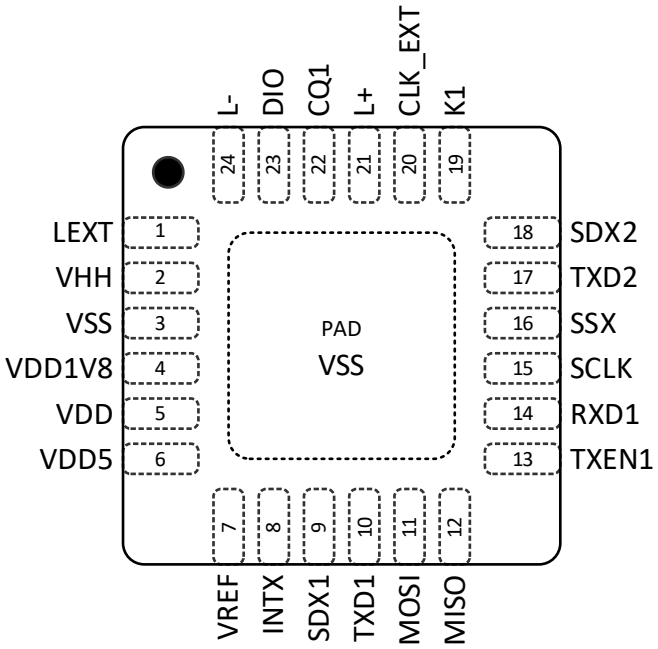


Figure 2: QFN24 Package (4x4mm, top view)

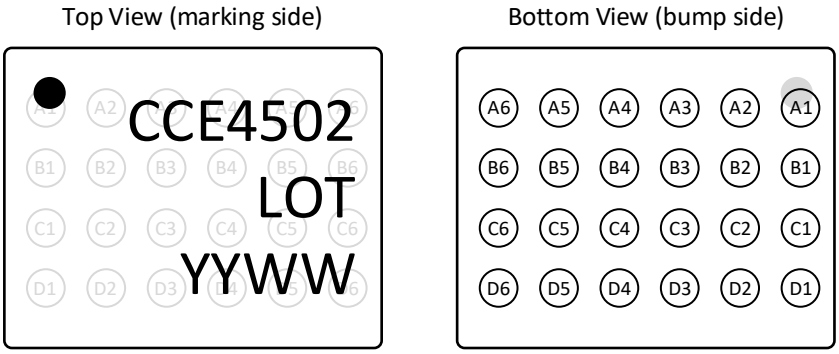


Figure 3: Chip Scale Package (top view, left, bottom view, right)

4.2. Pin Descriptions

Table 1: Pin Description

QFN24 Pin No	CSP Pin No	Name	Type	Power domain	Function	Remarks
1	D5	LEXT	PWR	VHH	DC/DC converter external inductance	
2	D4	VHH	PWR	VHH	Main supply / output DC/DC converter	
3, PAD	C4	VSS	PWR	-	Ground (Regulator)	

QFN24 Pin No	CSP Pin No	Name	Type	Power domain	Function	Remarks
4	D3	VDD1V8	PWR	VDD1V8	1.8 V Supply Voltage (Internal)	
5	C3	VDD	PWR	VDD	3.3/5 V Supply Voltage Output	
6	D2	VDD5	PWR	VDD5	5 V Supply Voltage Output	
7	D1	VREF	OUT	VDD	Reference Voltage	
8	C1	INTX	OUT	VDD	Interrupt output	Push-pull, active-low
9	C2	SDX1	OUT	VDD	Channel 1 short detection	Push-pull, active-low
10	B1	TXD1	IN	VDD	Channel 1 signal input	Internal pull up
11	A1	MOSI	IN	VDD	SPI Master Out/Slave In	Internal hold
12	B2	MISO	OUT	VDD	SPI Master In/Slave Out	Push-pull
13	A2	TXEN1	IN	VDD	Channel 1 driver enable	Internal pull down, active-high
14	B3	RXD1	OUT	VDD	Channel 1 signal output	Push-pull
15	A3	SCLK	IN	VDD	SPI Clock	Internal pull-down
16	B4	SSX	IN	VDD	SPI Slave Select	Internal pull-up
17	A4	TXD2	IN	VDD	Channel 2 signal input	Internal pull-up
18	A5	SDX2	OUT	VDD	Channel 2 short detection	Push-pull, low active
19	B5	K1	IN	VDD	Configuration bit 1	Internal pull down
20	A6	CLK_EXT	IN/OUT	VDD	External clock input / Clock output	Push-pull, Internal pull down
21	B6	L+	PWR	L+	Positive supply (IO-Link)	
22	C6	CQ1	IN/OUT	L+	IO-Link data channel 1	
23	D6	DIO	IN/OUT	L+	Switching Input / Output channel 2	
24	C5	L-	PWR	L+	Ground supply (IO-Link)	

5. Absolute Maximum Ratings

T_{amb} = 25 °C ± 1 °C unless otherwise specified.

Table 2: Absolute Maximum Ratings

No.	Parameter	Conditions	Name	Min	Typ	Max	Unit
A-01	Supply Voltage	Static, referenced to V_{L-}	V_{L+} -V_{L-}	-40		40	V
A-02	Supply Voltage	Dynamic, pulse width <= 100 ms, delay between pulses >= 100 s	V_{L+} -V_{L-} (pulse)	-50		50	V
A-03	VHH pad max voltage	Referenced to VSS	$V_{VHH,max}$	-0.3		(V_{L+} -V_{L-}) + 0.3 V	V
A-04	Power Dissipation	QFN24 Package on Multilayer PCB	P_{TOT}			1	W
A-05	Operating Temperature	Ambient temperature	T_{amb}	-40		105	°C
A-06	Storage Temperature		$T_{storage}$	-55		155	°C
A-07	Junction Temperature		T_j	-50		150	°C
A-08	Voltage at pin CQ1/DIO	Referenced to V_{L-}: V_{CQ}-V_{L-}	$V_{CQ,max}$	-0.3		(V_{L+} -V_{L-}) +0.3	V
A-09	Voltage at all other pins	Referenced to VSS	$V_{...max}$	-0.3		V_{DD} + 0.3	V
A-10	ESD protection	JS-001-2012 HBM	V_{ESD}	4			kV
A-11	Latch-up	JEDEC JESD78D Class1	$I_{latchup}$	100			mA
A-12	Soldering Temperature	12 s max.	T_{solder}			260	°C
A-13	FIT Rate	$T_{amb,max}$ = 70 °C				50	FIT

6. Electrical Characteristics

T_{amb} = -40 °C … 105 °C, VS = V_{L+}-V_{L-} = 24 V unless otherwise specified.

6.1. General Parameters

Table 3: General Parameters

No.	Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
G-01	Over temperature flag	$t_{deglitch}$=4096/fclk		T_{flag}	110	120	130	°C
G-02	Over temperature flag hysteresis			T_{hyst}	11		19	°C
G-03	Over voltage flag threshold	V_{L+} rising	21, 24	$V_{L+,thr+}$	38	40	42	V
G-04	Main Supply Voltage		21, 24	VS (V_{L+} -V_{L-})	9		36	V
G-05	LDO Input Voltage	DC/DC disabled (Supply Mode 2 or 3)	2,3	V_{VHH} - V_{VSS}	6		36	V
G-06	Supply voltage ripple	F_{ripple} = DC … 100 kHz	21	ΔV_{L+}			1.3	V_{p-p}
G-07	Quiescent Main Current	V_{L+} -V_{L-} = 24 V	21, 24	I_{L+}			10	mA
G-08	Quiescent LDO Current	V_{VHH} -V_{VSS} = 7 V	2, 3	I_{VHH}			2	mA
G-09	External capacitor VHH SM1	DC/DC enabled, ESR > 0.6 Ω	2, 3	$C_{VHH,DCDC}$	17.6			µF
G-10	External capacitor VHH SM2	DC/DC disabled (Supply Mode 2)	2, 3	C_{VHH}	100			nF
G-11	External capacitor VDD		5, 3	C_{VDD}	220	470		nF
G-12	External capacitor VDD5		6, 3	C_{VDD5}	47	100		nF
G-13	External capacitor VDD1V8	Between VDD1V8 and VSS	4, 3	C_{VDD1V8}	47	100		nF
G-14	Inductance DC/DC Converter		1, 2	L_{EXT}		22		µH
G-15	System clock frequency	T_{amb}=25 °C	20	F_{clk}	-2%	14.745	+2%	MHz
G-16	Reference Voltage	T_{amb}=25 °C, $I_{load,REF}$ < 100 uA	7, 3	V_{REF}	1.12	1.2	1.25	V
G-17	Reference Voltage Temperature Coefficient		7, 3	TK_{VREF}		80		ppm/K

6.2. 3.3V/5V Voltage Regulator

Table 4: Linear Regulator 3.3V / 5V

No.	Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
VD-01	Output Voltage VDD 5 V	CCE4502 configured to 5 V option, $C_{L+,L-}$ >= 10 µF	5, 3	VDD_{5V}	4.75	5	5.25	V
VD-02	Output Voltage VDD 3.3 V	CCE4502 configured to 3.3 V option, $C_{L+,L-}$ >= 10 µF	5, 3	VDD_{3V3}	3.1	3.3	3.5	V
VD-03	Voltage Drop VDD	Load Current = 25 mA	2, 5	V_{VHH}- V_{VDD}	0.7			V

No.	Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
VD-04	Output Current VDD		5	I_{VDD}			50	mA
VD-05	Line regulation VDD SM1/2	I_{VDD} = 10 mA, 9 V < V_{L+} < 36 V (Supply mode 1 and 2)	5, 3				10	mV
VD-06	Line regulation VDD SM3	I_{VDD} = 10 mA, 6 V < VHH < 36 V (Supply mode 3)					100	
VD-07	Load regulation VDD	DC current up to 50 mA	5, 3				1	%
VD-08	Power Supply Rejection Ratio VDD SM1/2	Supply mode 1+2 V_{L+}/V_{VDD}, C_{VHH} = 22 µF ESR > 0.6 Ω; C_{VDD} = 220 nF, f < 200 kHz	5, 3	PSRR	40			dB
VD-09	Power Supply Rejection Ratio VDD SM3	Supply mode 3 V_{VHH}/V_{VDD}, C_{VDD} = 220 nF, f < 200 kHz			40			dB
VD-10	Power-On Threshold VDD	Referenced to VDD target voltage (3.3 V or 5 V)	5, 3	V_{RST}	85	90	95	%
VD-11	Start-up time	After V_{L+} exceeds minimum value	5, 3	$t_{start-up}$			1	ms
VD-12	Start-up glitch blanking	Glitch blanking		t_{glf}		1		µs

6.3. 5V Voltage Regulator

Table 5: Linear Regulator 5V

No.	Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
V5-01	Output Voltage VDD5	$C_{L+,L-}$ >= 10 µF	6, 3	VDD5	4.75	5	5.25	V
V5-02	Voltage Drop VDD5	Load Current = 5 mA	2, 6	V_{VHH}-V_{VDD5}	0.7			V
V5-03	Output Current VDD5		6	I_{VDD5}			10	mA
V5-04	Line regulation VDD5	I_{VDD5} = 5 mA, 9 V < VL+ < 36 V	6, 3				10	mV
V5-05	Load regulation VDD5	DC current up to 5 mA	6, 3				0.2	%
V5-06	Power Supply Rejection Ratio VDD5	V_{L+}/V_{VDD5}, C_{VDD5} = 100 nF, f < 200 kHz		PSRR	40			dB

6.4. DC/DC Converter

Table 6: DC / DC Converter

No.	Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
DD-01	Output Voltage VHH	DC/DC in buck mode, $C_{L+,L-}$ >= 10 µF	2, 3	VHH_{DCDC}	6.5	7.2	7.9	V
DD-02	Output Voltage LEXT	DC/DC in linear mode, VHH and LEXT shorted	1, 3	$V_{LEXT,LDO}$	5.5	7	8.5	V
DD-03	Ripple VHH	L_{EXT} = 22 µH, C_{VHH} = 22 µF, ESR_{CVHH} > 0.6 Ω, I_{VHH} = 60 mA	2	$V_{VHH,pp}$			200	mV
DD-04	Switching Frequency DC/DC Converter	DC/DC in buck mode		f_{SWITCH}	1.5		2.5	MHz
DD-05	Output Current DC/DC Converter		2	$I_{DCDC,out}$			60*	mA
DD-06	Line regulation VHH	I_{VHH} = 1 mA, 9 V < V_{L+} < 24 V	2				10	%
DD-07	Load regulation VHH	DC current up to 25 mA	2, 3				1	%

6.5. Inputs / Outputs CQ1, DIO

Table 7: Switching Outputs

No.	Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
HV-01	Voltage CQ1/DIO		22, 23	V_{CQ_MAX}			36	V
HV-02	Output voltage low level CQ1/DIO	active pull down, I_{OL} = -200 mA	22, 23	V_{OL}			2	V
HV-03	Output voltage high level CQ1/DIO	active pull up, I_{OH} = +200 mA	22, 23	V_{OH}	V_S - 2			V
HV-04	Leakage current CQ1/DIO	input disabled	22, 23	I_{leak}	-100		100	µA
HV-05	Maximum Permanent Output Current CQ1/DIO	Current per CQ channel	22, 23	I_{CQmax}			200*	mA
HV-06	Output source current limit CQ1/DIO	SLEW = 0 (see section 7.8.5)	22, 23	I_{limP}			340	mA
HV-07	Output sink current limit CQ1/DIO		22, 23	I_{limN}			320	mA
HV-08	Overcurrent detection threshold CQ1/DIO	Source/sink current, SLEW = 0	22, 23	I_{OC}		210		mA
HV-09	Peak short circuit current CQ1/DIO	V_{L+} - V_L = 36 V Up to 1 µs after short	22, 23	$I_{short,peak}$			2	A
HV-10	Load capacitance CQ1/DIO	COM1 or COM2	22, 23	CL			5	nF
HV-11	Inductive load CQ1/DIO		22, 23	L_{Load}			50	mH
HV-12	Output slew rate rise/fall open CQ1/DIO	Open load, SLEW = 0	22, 23	$r_{slew,open}$	42	60	100	V/µs

* Consider devices total power consumption (see section 8.1).

No.	Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
HV-13	Output slew rate rise/fall 5nF CQ1/DIO	5 nF Load, SLEW = 0	22, 23	$r_{slew,5nF}$	20		40	V/µs
HV-14	Switch On Time CQ1/DIO		22, 23	t_{DLY_LH}			500	ns
HV-15	Switch Off Time CQ1/DIO		22, 23	t_{DLY_HL}			500	ns
HV-16	Break before Make Delay CQ1/DIO		22, 23	t_{LH_BBM}, t_{HL_BBM}	1		30	ns
HV-17	Short Circuit Detection Time CQ1/DIO	see H/V configuration register	22, 23	$t_{OVLDDET}$	100			µs
HV-18	Input threshold high level CQ1/DIO	CQ1/DIO	22, 23	V_{IH}	10.5		13	V
HV-19	Input threshold low level CQ1/DIO		22, 23	V_{IL}	8		11.5	V
HV-20	Hysteresis between input thresholds high and low CQ1/DIO		22, 23	V_{Hyst}	1			V

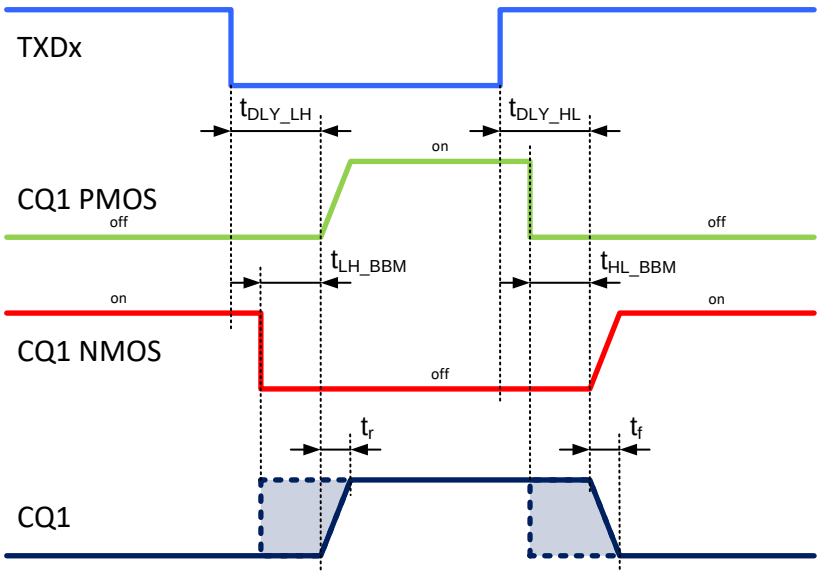


Figure 4: Timing CQ1 Outputs ("Break before Make")

The solid line of CQ1 signal in Figure 4 describes the typical or best case scenario. Depending on the external circuitry, the slew rate can differ from this. This is shown by the shaded area e. g. an external pull-up pulls CQ1 high as soon as the NMOS is switched off.

6.6. IO-Link Protocol

Table 8: IO-Link specification

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Transmission rate	COM1 COM2 COM3		f_{DTR}		4,8 38,4 230,4		kbit/s

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Bit time	COM1 COM2 COM3		T_{BIT}		208,3 26,0 4,34		µs
UART frame transmission delay of the Device			T_{dD}	0		3	T_{BIT}
Response time of Devices			T_{Dev_resp}	1		10	T_{BIT}
Cycle time	M-sequence Type_2_1 COM1 COM2 COM3		T_{CYC}	 18 2,3 0,4			ms

6.7. Digital I/O

Table 9: Digital Inputs

No.	Parameter	Conditions	Name	Min	Typ	Max	Unit
DI-01	Input Voltage LOW 3.3 V digital I/O	V_{DD} - V_{SS} = 3.3 V	$V_{IN\_L\_3V3}$			1.5	V
DI-02	Input Voltage HIGH 3.3 V digital I/O	V_{DD} - V_{SS} = 3.3 V	$V_{IN\_H\_3V3}$	1.8			V
DI-03	Input Voltage LOW 5 V digital I/O	V_{DD} - V_{SS} = 5.0 V	$V_{IN\_L\_5V}$			2.1	V
DI-04	Input Voltage HIGH 5 V digital I/O	V_{DD} - V_{SS} = 5.0 V	$V_{IN\_H\_5V}$	2.9			V
DI-05	Input Capacitance digital I/O		C_{IN}			5	pF
DI-06	Input Leakage Current digital I/O		I_{ILEAK}	-5		5	µA
DI-07	Input Pull-Up current 3.3 V digital I/O	V_{DD} - V_{SS} = 3.3 V, V_{pin} = 0 V	I_{PU_3V3}	10		40	µA
DI-08	Input Pull-Up current 5 V digital I/O	V_{DD} - V_{SS} = 5.0 V, V_{pin} = 0 V	I_{PU_5V}	25		100	µA
DI-09	Input Pull-Down current 3.3 V digital I/O	V_{DD} - V_{SS} = 3.3 V, V_{pin} = 3.3 V	I_{PD_3V3}	20		70	µA
DI-10	Input Pull-Down current 5 V digital I/O	V_{DD} - V_{SS} = 5.0 V, V_{pin} = 5.0 V	I_{PD_5V}	20		70	µA

Table 10: Digital Outputs

No.	Parameter	Conditions	Name	Min	Typ	Max	Unit
DO-01	Output Voltage LOW 3.3 V digital I/O	V_{DD} - V_{SS} = 3.3 V I_{OUT_LOW} = 2 mA	V_{OUT_L}			0.5	V
DO-02	Output Voltage LOW 5 V digital I/O	V_{DD} - V_{SS} = 5.0 V I_{OUT_LOW} = 2 mA	V_{OUT_L}			0.5	V
DO-03	Output Voltage HIGH 3.3 V digital I/O	V_{DD} - V_{SS} = 3.3 V I_{OUT_HIGH} = 2 mA	V_{OUT_H}	2.8			V
DO-04	Output Voltage HIGH 5 V digital I/O	V_{DD} - V_{SS} = 5.0 V I_{OUT_HIGH} = 2 mA	V_{OUT_H}	4.5			V
DO-05	Output Leakage Current digital I/O	Tristate active	I_{OLEAK}	-5		5	µA

No.	Parameter	Conditions	Name	Min	Typ	Max	Unit
DO-06	Output Capacitance digital I/O		C_{OUT}		5		pF

7. Functional Description

7.1. Overall Functional Description

The IC integrates one IO-Link capable bidirectional switching interface connected to CQ1. It can be used as a SIO, UART transceiver or IO-Link slave port. It includes a hardware IO-Link frame handler based on the UART interface, which provides IO-Link protocol handling facilities. The pin DIO is configured as an output. Both pins, CQ1 and DIO, are individually configured as push-pull, open drain (PMOS or NMOS) or input only.

The CCE4502 is controlled via IO pins or the SPI.

An integrated oscillator provides the core logic clock. Alternatively, an external 14.745 MHz clock can be provided at pin CLK_EXT.

7.2. Protection Circuitry

The CCE4502 has following protection circuitry:

1. All pins are protected against ESD.
2. The CQ1 and DIO outputs, the L+ and L- Pins are protected against reverse polarity connections according to Table 11.
3. CQ1 and DIO output transistors are protected against overcurrent.
4. On-chip over temperature is detected and notified.

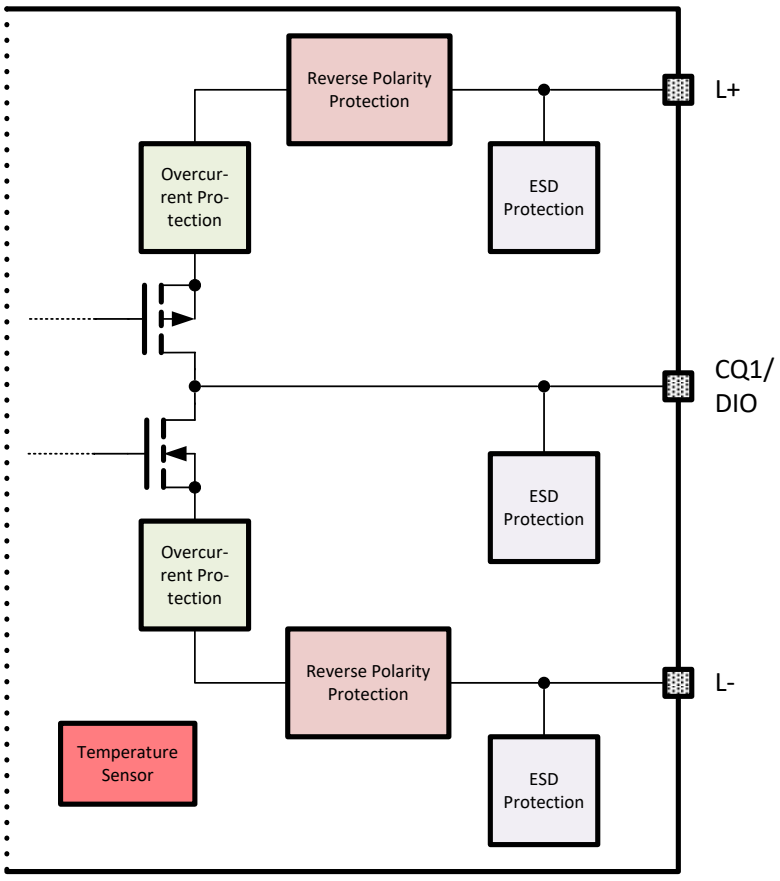


Figure 5: Protection circuitry at CQ1, DIO, L+ and L-

Table 11: Allowed reverse polarity connections

Case	L-	L+	CQ1/DIO	Remark
1	0	1	0	Regular connection (output shorted to ground)
2	0	1	1	Regular connection (output shorted to Plus)
3	0	1	H	Regular connection (output open)
4	H	1	0	Missing ground (IC get current by output)
5	0	H	1	Missing Plus (IC get current by output), see notes below
6	1	0	1	Reverse polarity (output shorted to Plus)
7	1	0	H	Reverse polarity (output open)
8	H	0	1	Missing ground (IC get current by output)
9	1	0	0	Reverse polarity (output shorted to ground)
10	1	H	0	Missing Plus (IC get current by output)

Notes to Table 11:

- “0” means connected to ground
- “1” means connected to Plus (VS)
- “H” means connection left open
- Non–regular connection means the IC will not operate
- In case of a non-regular connection either CQ1 or DIO has to be left open
- In case of reverse polarity case 5 the channel connected to supply must not drive low (0 V) and L+ must not be connected to any loads. Any connected microcontroller should be inactive.

7.3. Power Supply

The CCE4502 implements five regulators for the power supply of the IC and external components.

1. A DC/DC converter at pin LEXT/VHH is permanently configured for either buck mode or linear regulation mode by factory setup (see ordering information). This converter may supply external circuitry.
2. A linear regulator with output at pin VDD, which is permanently configured for 3.3V or 5V output voltage by factory setup (see ordering information), and can supply external circuitry.
3. A 5V linear regulator with output at pin VDD5. This regulator may supply external circuitry.
4. A 1.8V core supply regulator with output at pin VDD1V8. External load must not be connected to pin VDD1V8.
5. A buffered reference voltage of 1.2V is provided at pin VREF.

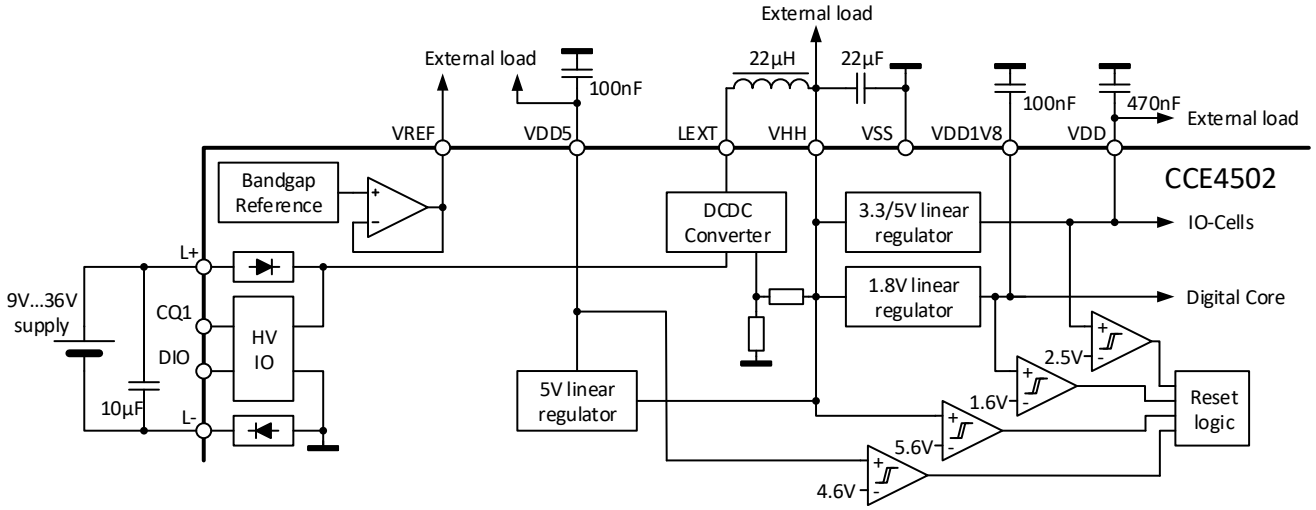


Figure 6: Power supply block diagram. DC/DC converter in switch mode (Supply Mode 1)

Note 1 Always calculate the maximum IC junction temperature to decide if the IC can supply the required currents for external circuitry. In particular, the IO-Link output stage currents, LDOs supply currents and thermal coupling of the IC to the PCB will affect the junction temperature.

7.3.1. DC / DC Converter, Supply Modes

A DC/DC converter is provided which either acts as a buck mode switching converter, requiring an external inductor, or as a linear regulator. The function of the converter is factory programmed (see Ordering Information).

7.3.1.1. Supply Mode 1 – DC/DC converter in buck mode

The main purpose of the buck converter mode is to limit the on-chip power dissipation by converting the main supply voltage at L+ and L- to an intermediate level of about 7V. See Figure 6 and Figure 13 for the recommended application schematic in this supply mode.

The output of the buck converter can be used to drive external circuitry connected to pin VHH. In total, the external load current must not exceed 60mA at VHH and VDD. The buck converter is designed for an external 22µH inductor between pins LEXT and VHH. The inductor's saturation current must higher than 300mA.

A 22µF capacitor is required between pins VHH and VSS to buffer the buck converters output. The ESR of this capacitor must be higher than 0.6Ω. This may require a 0.6Ω resistor in series to the 22µF capacitor.

A 10µF capacitor is recommended between L+ and L-.

7.3.1.2. Supply Mode 2 – DC/DC converter in linear regulator mode

If the DC/DC converter is configured for linear regulation mode, it provides about 7V at LEXT. LEXT and VHH must then be shorted externally. See Figure 14 for the recommended application schematic in this supply mode.

7.3.1.3. Supply Mode 3 – DC/DC converter not used

If the DC/DC converter is not required by the application, leave pin LEXT floating. The 3.3V/5V and 1.8V regulators must then be supplied by an external 6V to 36V supply connected to pin VHH.

It is recommended to use devices with factory configuration "linear mode" if supply mode 3 is used.

See Figure 15 for the recommended application schematic in this supply mode.

7.3.2. VDD – 3.3V / 5V Linear Regulator

The 3.3 V / 5 V regulator provides power for all logic level in- and outputs (pins 8 to 20) at pin VDD. The output voltage (3.3 V or 5 V) is permanently set during the final test of the IC. See section 11 for corresponding order codes.

A capacitor with at least 220 nF from pin VDD to VSS is required for stable regulator operation and provides a buffer for currents spikes of switching digital outputs.

The regulator input is connected to VHH, which can be supplied by the on-chip DC/DC converter or an external supply. See Figure 13, Figure 14 and Figure 15 for possible connection options.

The LDO output can supply external circuitry (e. g. microcontrollers). In total, the external load current must not exceed 50 mA. Always calculate that the ICs junction temperature does not exceed specified limits, when using the regulator outputs for external load.

7.3.3. VDD1V8 – 1.8V Linear Regulator

The 1.8 V regulator provides power for internal logic blocks. A 100 nF capacitor from pin VDD1V8 to VSS is required. Do not connect external load to pin VDD1V8.

7.3.4. VDD5 – 5V Linear Regulator

A 5 V regulator provides power for internal and external circuitry at pin VDD5. The regulator input is connected to VHH, which can be supplied by the on-chip DC/DC converter or an external supply. See Figure 13, Figure 14 and Figure 15 for possible connection options. A 100nF capacitor from pin VDD5 to VSS is recommended. External load connected to VDD5 must not draw more than 10mA.

7.3.5. VREF – Reference Voltage Output

An internal bandgap circuit provides a reference voltage at pin VREF. External load current at pin VREF must not exceed 100µA.

7.4. Power-On Reset

The power on reset circuitry supervises the main (L+/L-), IO (3.3V/5V) and core (1.8 V) supplies to ensure proper initialization of all registers (see Figure 6). If the internal power on reset signal is activated, the logic core is reset to defaults and all outputs are in high impedance state.

A glitch filter is implemented to suppress supply voltage sags shorter than t_{glf}. See Figure 7.

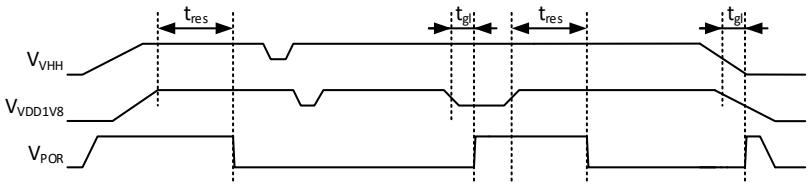


Figure 7: Power-On Reset timing (only core voltage 1.8V POR depicted)

7.5. Configuration Pin K1

The configuration pin K1 defines whether the internal or an external oscillator is used to clock the core logic. If an external clock is used the internal clock generator is disabled. Table 12 lists configuration options. Connect pin K1 to VSS or leave it unconnected to use the internal oscillator.

Table 12: K1 Configuration Bit

K1	CLK_EXT	Functional Mode
VSS	Output	Functional Mode using internal oscillator (default)
VDD	Input	Functional Mode using external crystal oscillator

7.6. HV-IO Stages

Two identical output stages drive the channel 1 and channel 2 pins (CQ1/DIO). Each output transistor pair has individual slew rate control and current limiting circuitry. The output slew rate, output current limit and output overcurrent detection threshold can be adjusted for each channel via the SLEW1/2 registers (7.8.5). The control logic is shown in Figure 8.

Channel 1 provides an input buffer compatible to the IO-Link standard. The input buffer can be disabled via the CONF1.DIS register. See Table 13.

Table 13: Channel 1 input buffer truth table

CQ1	CONF1.DIS	RXD
High	0	0
Low	0	1
X	1	1

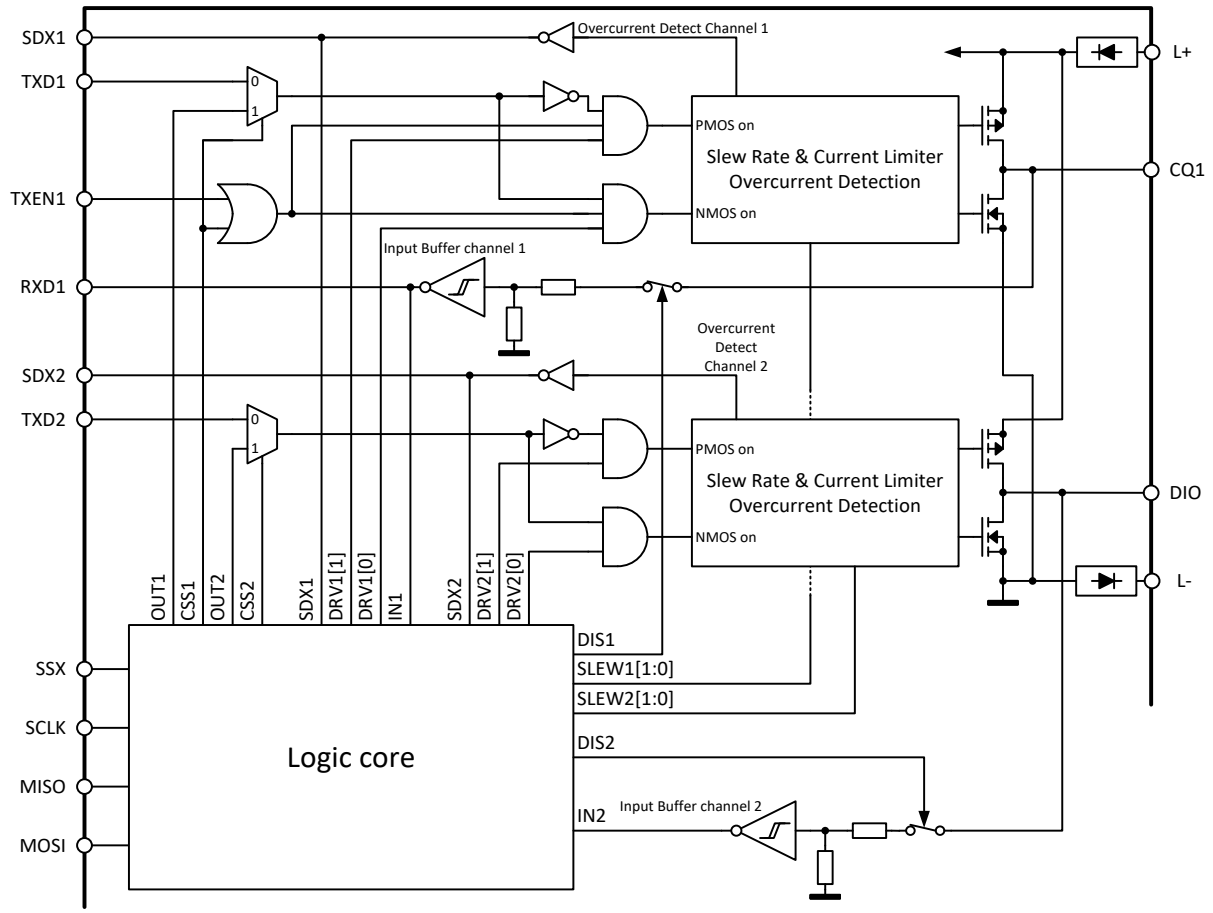


Figure 8: HV-Output stage

If the output current of channel 1 or channel 2 exceeds the output current limit defined via the SLEW1/2 registers (7.8.5), an overcurrent detection signal is available at SDX1 and SDX2 respectively. The logic core also receives this information and disables the output stages if configured in OVLD1/2 registers (see 7.8.4).

Table 14: Overcurrent detection truth table

Output state	SDXx
Output current below overcurrent detection threshold	1
Output current above overcurrent detection threshold	0

Each channel can be controlled either by dedicated control pins (TXD1, TXEN1, TXD2) or the SPI interface. The registers CONF1.CSS (7.8.2) CONF2.CSS (7.8.3) define if the outputs are controlled by the dedicated pins or SPI. This allows the IC to be used as level shifter only, without using the SPI interface.

The logic core defines the configuration of the output stages (High-Z, Open-Drain, Push-Pull) via the CONF1.DRV 7.8.2) and CONF2.DRV 7.8.3) registers. Default values of these registers are programmed during final test of the IC. A One-Time-Programmable memory element is used to store this information. The memory content cannot be changed after the ICs final test. Changing the CONF1 and CONF2 registers in the application requires SPI access.

To control the output stages via SPI only, the registers CSS1 and CSS2 must be set to one, thus ignoring the dedicated control pins (TXD1, TXEN1, TXD2). See Table 15 and Table 16 for the full output stages logic.

Table 15: Channel 1 output stage truth table

TXEN1	TXD1	CONF1.CSS	SIO1.OUT	CONF1.DRV[1:0]	CQ1
1	0	0	X	0	High-Z
1	0	0	X	1	High-Z
1	0	0	X	2	High
1	0	0	X	3	High
1	1	0	X	0	High-Z
1	1	0	X	1	Low
1	1	0	X	2	High-Z
1	1	0	X	3	Low
0	X	0	X	X	High-Z
X	X	1	0	0	High-Z
X	X	1	0	1	High-Z
X	X	1	0	2	High
X	X	1	0	3	High
X	X	1	1	0	High-Z
X	X	1	1	1	Low
X	X	1	1	2	High-Z
X	X	1	1	3	Low

Table 16: Channel 2 output stage truth table

TXD2	CONF2.CSS	SIO2.OUT	CONF2.DRV[1:0]	DIO
0	0	X	0	High-Z
0	0	X	1	High-Z
0	0	X	2	High
0	0	X	3	High
1	0	X	0	High-Z

TXD2	CONF2.CSS	SIO2.OUT	CONF2.DRV[1:0]	DIO
1	0	X	1	Low
1	0	X	2	High-Z
1	0	X	3	Low
X	1	0	0	High-Z
X	1	0	1	High-Z
X	1	0	2	High
X	1	0	3	High
X	1	1	0	High-Z
X	1	1	1	Low
X	1	1	2	High-Z

7.7. Operational Modes

There are three possible operational modes for channel1 – Standard I/O, UART and Frame Handler (IO-Link*) Mode. The channel mode can be configured via the MODE-bits of the CONF1 register (see 7.8.2). Channel 2 is always in Standard I/O mode. The desired output driving mode, i. e. N, P or Push-Pull driving, can be configured via the DRV-bits of the CONF1/2 register.

7.7.1. Standard I/O (SIO)

If a channel is configured in the Standard I/O Mode, the output driver can be directly controlled via the OUT-bit of register SIO1/2 (7.8.6 and 7.8.7). The IO-bit of SIO1 reflects the current state of the CQ1 pin.

In this mode, it is also possible to control and observe the channel using the TXD1/2, TXEN1 and RXD1 pins. To distinguish between pin- and logic-control, the Channel-Source-Select-bit (CSS) of register CONF1/2 has to be set accordingly.

Since the sense of TXD1/2 to CQ is inverted, it is possible to connect a standard microcontroller UART interface with a high idle state to the TXD/RXD pins.

7.7.2. UART

The UART mode of channel 1 is designed to send and receive 8 bits of data per character followed by an even parity bit. If this mode is enabled the used COM speed needs to be set in the CONF1 register.

By default, the channel will listen for incoming UART transactions at the CQ1 pin. If a character is received, an interrupt is triggered and the data can be read back from the UART register (7.8.8). A transaction is started by writing the data to the UART register.

The received UART data is not buffered. Receiving multiple characters, while not reading them back, causes data loss. This will be indicated by the OFLW-bit in the STAT-register 7.8.18).

7.7.3. Frame Handler (IO-Link Mode)

The Frame Handler Mode extends the UART interface. It is required to define the used COM speed in the CONF1 register.

The frame handler mostly automates the transceiving of M-sequences as defined by the IO-Link protocol. It buffers frames of incoming master messages and outgoing device messages in its internal frame buffer. The buffer can be accessed by reading or writing the register FHD (7.8.14). The CRC checksums of all incoming messages are automatically checked. Any UART parity bit errors and CRC errors are indicated. For outgoing messages, the CRC checksums are automatically calculated and inserted into the messages.

* IO-Link Interface and System Specification, Version 1.1.2, July 2013

The frame handler monitors the specified timing constraints of the IO-Link standard and takes care to comply with them as well. These constraints are the delay between UART frames in the device message, the delay between UART frames in the master message, and the response time between master message and device message. A violation of any of these constraints is detected as a timeout.

7.7.3.1. Configuration

The length of each message is influenced by the ODL, MPDL and DPDL registers. It also depends on the access type, addressed channel and M-sequence type which is defined in the second byte of each M-sequence. M-sequences of type 0 (FT0) always use one byte on-request data. M-sequences of type 1 (FT1) use the MPDL or DPDL lengths, if the address channel is the Process Data Channel; otherwise the ODL length is used. M-sequences of type 2 (FT2) always use the MPDL, DPDL and ODL lengths (see Figure 9).

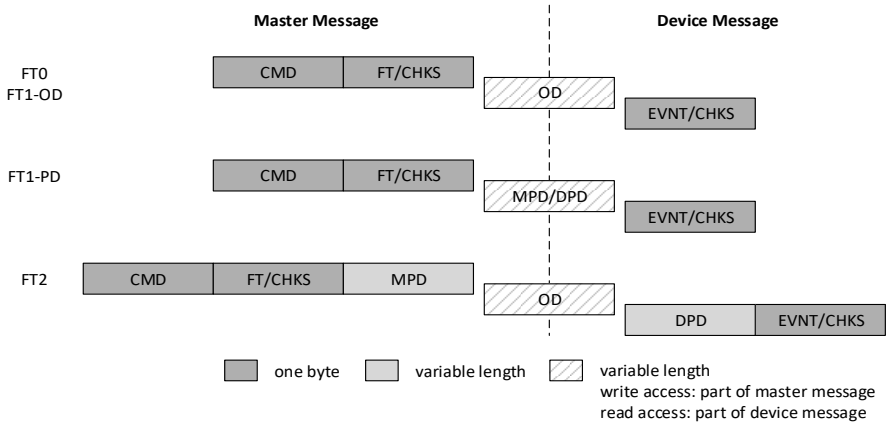


Figure 9: M-sequences of different types

7.7.3.2. Operation

The frame handler listens for incoming master messages and triggers an interrupt if a part or the complete message is received. The interrupt behavior can be modified using the INT_EN_FH (7.8.26) and TRSH (7.8.15) register. The received data can be read back via the FHD register (7.8.14) by multiple SPI transactions or single/multiple bulk SPI transactions.

After successfully receiving an incoming master message, the frame handler waits for the user to write the complete device message data into the frame buffer via the FHD register, including the CHKS byte. The access to the FHD register can be done by multiple SPI transactions or by a single bulk SPI transaction. The six least significant bits of the CHKS byte are automatically replaced with the compressed checksum of the device message. The UART transmission always starts immediately after the first byte is written into the frame buffer.

It is possible to reset the frame handler or skip an invalid M-sequence from any state. This can be done by writing ‘1’ to the RST- or SKIP-bit of the FHC register 7.8.9). Skipping a M-sequence causes the frame handler to ignore the rest of an incoming message, without triggering any additional interrupt. Another way to alter the operational flow is a soft reset. A soft reset is done after receiving the rest of the invalid message or if a timeout was detected. A soft reset will immediately reset the frame handler to its idle state.

The state diagram of the frame handler is depicted in Figure 10.

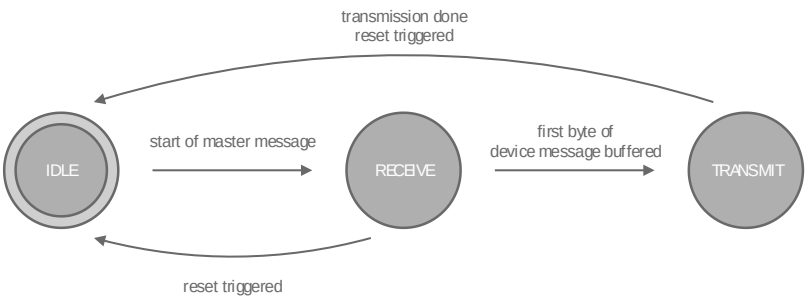


Figure 10: Frame handler state diagram

7.8. Register Description

Registers are used to configure the ICs behavior. These registers can be read or written via the SPI interface. They are divided into three functional groups:

1. The logic connected to pin CQ – also referred to as channel 1
2. The logic connected to pin DIO – also referred to as channel 2
3. General purpose.

7.8.1. Register Definitions

Table 17: Register Definitions

Address	Name	Description
0x00-0x1F	-	reserved
Channel 1 Regs		
0x20	CONF1	Channel Configuration
0x21	OVLD1	Overload Protection
0x22	SLEW1	Slew Rate Control
0x23	SIO1	SIO Control
0x24	UART	UART Data
0x25	FHC	Frame Handler Control
0x26	ODL	On-Request Data Length
0x27	MPDL	Master Process Data Length
0x28	DPDL	Device Process Data Length
0x29	BLVL	Frame Handler Buffer Level
0x2A	FHD	Frame Handler Data
0x2B	-	reserved (must not be used by future regs)
0x2C-0x2D	-	reserved
0x2E	TRSH	Threshold Level Interrupt Triggering
0x30-0x3F	-	reserved
Channel 2 Regs		
0x40	CONF2	Channel Configuration
0x41	OVLD2	Overload Protection
0x42	SLEW2	Slew Rate Control
0x43	SIO2	SIO Control
0x44 – 0x5F	-	reserved
Common Regs		
0x60	REV	Revision Code
0x61	PROT	Channel Protection
0x62	STAT	Channel Status
0x63	INT_SRC_STAT	Status Interrupt sources

Address	Name	Description
0x64	INT_EN_STAT	Status Interrupt enables
0x65	INT_SRC_SIO	Interrupt sources of SIO-mode
0x66	INT_EN_SIO	Interrupt enables of SIO-mode
0x67	INT_SRC_UART	Interrupt sources of UART-mode
0x68	INT_EN_UART	Interrupt enables of UART-mode
0x69	INT_SRC_FH	Interrupt sources of FH-mode
0x6A	INT_EN_FH	Interrupt enables of FH-mode
0x6B	-	reserved
0x6C	CLK_OUT	Output-Clock control
0x6D – 0x7F	-	reserved

7.8.2. CONF1 Register (0x20)

This is the configuration register for IO-Link-channel 1. It is possible to configure the channel mode and the communication speed used by the integrated UART, or to generally disable the input stage. Further the channel source and the output stage type can be configured. The output stage can be configured as P-, N-Mode or Push-Pull.

Table 18: CONF1 register

Bit	7	6	5	4	3	2	1	0
Name	DIS	DRV		CSS	COM		MODE	
Access	R/W	R/W		R/W	R/W		R/W	
Default	0	11b		0	0		0	

MODE *Channel Mode*

0h: SIO Mode (default)
1h: UART Mode
2h: Frame Handler (IO-Link) Mode
3h: reserved

COM *UART communication mode*

0h: UART disabled (default)
1h: COM1 (4.8 kBit/s)
2h: COM2 (38.4 kBit/s)
3h: COM3 (230.4 kBit/s)

CSS *Channel Source Select*

0: Channel inputs TXD1 and TXEN_1 are controlled via pins
1: Channel inputs TXD1 and TXEN_1 are controlled via internal logic core

DRV *Output stage configuration*

00b CQ1 disabled
01b N-Mode

10b P-Mode
11b Push-Pull

DIS *IO-Link input stage disable*

0: Input stage enabled
1: Input stage disabled (RXD1 = 1)

7.8.3. CONF2 (0x40)

This is the configuration register for channel 2. The channel source and the output stage type can be configured. The output stage can be configured as P-, N-Mode or Push-Pull.

Table 19: CONF2 register

Bit	7	6	5	4	3	2	1	0
Name	DIS	DRV		CSS	reserved			
Access	R/W	R/W		R/W	-			
Default	0	11b		0	-			

CSS *Channel Source Select*

0: Channel input TXD2 is controlled via pins
1: Channel input TXD2 is controlled via internal logic core

DRV *Output stage configuration*

00b DIO disabled
01b N-Mode
10b P-Mode
11b Push-Pull

DIS *IO-Link input stage disable*

0: Input stage enabled
1: Input stage disabled

7.8.4. OVLD 1 / 2 (0x21 / 0x41)

This is the configuration register for the detection of a high channel load. The detection time of high load and the corresponding disable time of a channel can be configured. If the automatic channel disable function is active and an overcurrent condition at this channel is present for $t_{OVLDDET}$, the channel gets disabled. After $t_{OVLDDIS}$ passed, the channel is enabled again.

$t_{OVLDDET}$ = 100us * (1 + MULT)

$t_{OVLDDIS}$ = 100us * (1 + MULT) * FACTOR

CAUTION: Disabling this feature may cause damage to the device!

Table 20: OVLD register

Bit	7	6	5	4	3	2	1	0
Name	ADIS		MULT					
Access	R/W		R/W					
Default	11b		000000b					

ADIS *Automatic Channel Disable*

0h: disabled
1h: enabled, FACTOR is 10
2h: enabled, FACTOR is 100
3h: enabled, FACTOR is 1000

MULT *Multiplier Value*

7.8.5. SLEW 1 / 2 (0x22 / 0x42)

This is the slew rate control register for the IO-Link device.

Table 21: SLEW register

Bit	7	6	5	4	3	2	1	0
Name	Reserved						SLEW	
Access	-						R/W	
Default	-						0	

SLEW *CQ Output slew rate, current limit and overcurrent detection threshold*

0h: Slew rate: 60V/µs	Current limit: 300mA	Overcurrent threshold: 210mA
1h: Slew rate: 30V/µs	Current limit: 150mA	Overcurrent threshold: 105mA
2h: Slew rate: 20V/µs	Current limit: 100mA	Overcurrent threshold: 70mA
3h: Slew rate: 15V/µs	Current limit: 75mA	Overcurrent threshold: 53mA

(default: 0h)

7.8.6. SIO1 (0x23)

This register controls the IO-Link-channel (channel1) if it is configured in SIO mode. Please note the inverted logic!

Table 22: SIO1 register

Bit	7	6	5	4	3	2	1	0
Name	Reserved						IN	OUT
Access	-						R	R/W
Default	-						0	0

OUT *CQ1* *Driver Output Value*

0b Set CQ1 to high level
1b Set CQ1 to low level

IN *Status of Pin CQ1*

0b Pin CQ1 is at high level
1b Pin CQ1 is at low level

7.8.7. SIO2 (0x43)

This register controls the output and can read the input at the pin DIO. Please note the inverted logic!

Table 23: SIO2 register

Bit	7	6	5	4	3	2	1	0
Name	Reserved						IN	OUT
Access	-						R	R/W
Default	-						0	0

OUT *DIO Driver Output Value*

0b Set DIO to high level
1b Set DIO to low level

IN *Status of Pin DIO*

0b Pin DIO is at high level
1b Pin DIO is at low level

7.8.8. UART (0x24)

If channel1 is configured in UART mode, reading this register returns a received UART character. Writing to this register sends the given character using the integrated UART.

Table 24: UART register

Bit	7	6	5	4	3	2	1	0
Name	DATA (UART_TX write / UART_RX read)							
Access	R/W							
Default	00h							

DATA *UART character*

7.8.9. FHC (0x25)

This register is used to configure and control the behaviour of the frame handler (IO-Link mode) of channel 1.

Table 25: FHC register

Bit	7	6	5	4	3	2	1	0
Name	RST	SKIP	Reserved			CONF_FDEL		TOUT
Access	W	W	-			R/W		R/W
Default	0	0	0h			0h		0

TOUT *Set this bit to relax each timing constraint by +3TBIT*

CONF_FDEL *Adjust delay between UART frames of device message (inter-frame-delay)*
(field is not available in versions CB, CC, CD)

0h Minimum inter-frame delay (almost 0 TBIT)
1h Inter-frame delay set to 0.25 TBIT
2h Inter-frame delay set to 0.5 TBIT
3h Inter-frame delay set to 1 TBIT

SKIP *Skip current frame (Note: while writing to this bit, other register values won't be changed)*

RST *Reset frame handler (Note: while writing to this bit, other register values won't be changed)*

7.8.10. ODL (0x26)

This register configures the length of the on-request data in bytes. According to the IO-Link specification, valid values are 1, 2, 8 or 32. (Note: Writing to this register causes a reset of the frame handler.)

Table 26: ODL register

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							
Default	01h							

LEN *On-Request Data Length*

7.8.11. MPDL (0x27)

This register configures the length of the master process data in bytes. Valid values are 0-32. (Note: Writing to this register causes a reset of the frame handler.)

Table 27: MPDL register

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							
Default	00h							

LEN *On-Request Data Length*

7.8.12. DPDL (0x28)

This register configures the length of the device process data in bytes. Valid values are 0-32. (Note: Writing to this register causes a reset of the frame handler.)

Table 28: DPDL register

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							
Default	00h							

LEN *On-Request Data Length*

7.8.13. BLVL (0x29)

This register returns the current fill level of the frame handlers input buffer. This can be used for bulk access to the FHD register.

Table 29: BLVL register

Bit	7	6	5	4	3	2	1	0
Name	FCNT							
Access	R							
Default	00h							

FCNT *Fill count of the frame handlers input buffer*

7.8.14. FHD (0x2A)

If channel1 is configured in IO-Link mode, reading this register returns the buffered UART characters of a received message. Writing to this register buffers the given characters for an outgoing message (via a ringbuffer), which gets sent over the integrated UART.

Table 30: FHD register

Bit	7	6	5	4	3	2	1	0
Name	DATA							
Access	R/W							
Default	-							

DATA *Message character*

7.8.15. TRSH (0x2E)

This register is used to set a threshold level which is used for level interrupt triggering. (see 7.8.25)

Table 31: TRSH register

Bit	7	6	5	4	3	2	1	0
Name	Reserved		LVL					
Access	-		R/W					
Default	-		00h					

LVL *Threshold for level interrupt triggering (after TLVL received characters)*

7.8.16. REV (0x60)

This register contains the CCE4502 revision code.

Table 32: REV register

Bit	7	6	5	4	3	2	1	0
Name	MAJ				MIN			
Access	R				R			
Default	7h				0h			

MAJ *Major revision code*

MIN *Minor revision code*

7.8.17. PROT (0x61)

This channel protection register controls if the IO-Link channel should become disabled by on chip high temperature or high VCC voltage protection. (NOTE: disabling this function may cause damage to master and/or device)

Table 33: PROT register

Bit	7	6	5	4	3	2	1	0
Name	Reserved					PTEMP	PVCCH	Reserved
Access	-					R/W	R/W	-
Default	-					1b	1b	-

PTEMP *Channel disable on over temperature*

0b Channel is not disabled if over-temperature was flagged
1b Channel is disabled if over-temperature was flagged

PVCCH *Channel disable on over voltage*

0b Channel is not disabled if over-voltage was flagged
1b Channel is disabled if over-voltage was flagged

7.8.18. STAT (0x62)

This register contains some status information depending on the current mode that channel 1 is in. Bit 4 can be used to check if the chip has gone through a factory reset.

Table 34: STAT register

Mode	Bit	7	6	5	4	3	2	1	0
SIO		Reserved			TEST_ FACTORY_ RESET	WURQ	RXD	OUT2	OUT1
UART						OFLW	RXERR	RXRDY	TXRDY
FH						TOUT	STATE		
Access					R/W	R	R	R	R
Default					0	0	x	0	0

OUT1 *Channel output value*

0b CQ1 is driven high
1b CQ1 is driven low

OUT2 *Channel output value*

0b DIO is driven high
1b DIO is driven low

RXD Input state

0b High level detected at input CQ1
1b Low level detected at input CQ1

WURQ Internal wakeup request detection pulse which is reset at the end of any following SPI access

0b No wakeup request (IO-Link) received
1b Wakeup request (IO-Link) received

TXRDY UART Transmit state

0b UART is busy transmitting
1b UART is ready to send

RXRDY UART receive state

0b UART is ready to receive new data
1b New Data is available in UART

RXERR UART parity error flag

0b Last byte was received without parity error
1b Last byte received with parity error

OFLW UART receive buffer overflow

0b No receive buffer overflow
1b UART received byte, but receive buffer was not empty

STATE Frame Handler state (see section 7.7.3)

000b IDLE
001b Transmission inactive; frame handler waits for data at register FHD
010b Transmission active; no further data required
011b Transmission active; frame handler waits for data at register FHD
100b Receiving active
101b Receiving active; new input available, read register FHD
110b Receiving active; received message is erroneous
111b Receiving active; received message is erroneous; new input available, read register FHD

TOUT Frame handler timeout (see section 7.7.3)

0b No timeout detected
1b Timeout detected

TEST_FACTORY_RESET (field is not available in versions CB, CC, CD)

This Bit can be set to ‘1’ via SPI and will be reset to ‘0’ after a hardware reset. It has no effect on the functionality of the chip, but can be used to check whether the digital core has gone through a reset.

7.8.19. INT_SRC_STAT (0x63)

The status interrupt-source-register contains various relevant status information of the IC. All bits are set by hardware. An interrupt is generated if at least one of these bits is enabled via INT_EN_STAT and contains a ‘1’. Writing a ‘1’ to either of these bits clears this interrupt-source individually. Writing a ‘0’ to any of these bits has no effect.

Table 35: INT_SRC_STAT register

Bit	7	6	5	4	3	2	1	0
Name	Reserved	HIGH_T	HIGH_VS	Reserved	CH_DIS2	CH_DIS1	SD2	SD1
Access	-	R/W1	R/W1	-	R/W1	R/W1	R/W1	R/W1
Default	-	0	0	-	0	0	0	0

SD1/2 *Short detected at pin CQ1 and DIO*

CH_DIS1/2 *Channel CQ1 and DIO disabled due to a detected overload*

HIGH_VS *High voltage detected*

HIGH_T *High temperature detected*

7.8.20. INT_EN_STAT (0x64)

The status interrupt-enable-register allows the user to enable each status interrupt-source individually.

Table 36: INT_EN_STAT register

Bit	7	6	5	4	3	2	1	0
Name	-	HIGH_T_EN	HIGH_VS_EN	-	CH_DIS2_EN	CH_DIS1_EN	SD2_EN	SD1_EN
Access	-	R/W	R/W	-	R/W	R/W	R/W	R/W
Default	-	0	0	-	0	0	0	0

SD1/2_EN *Enables the interrupt source SD* *(0b: disabled 1b: enabled)*

CH_DIS1/2_EN *Enables the interrupt source CH_DIS* *(0b: disabled 1b: enabled)*

HIGH_VS_EN *Enables the interrupt source HIGH_VS* *(0b: disabled 1b: enabled)*

HIGH_T_EN *Enables the interrupt source HIGH_T* *(0b: disabled 1b: enabled)*

7.8.21. INT_SRC_SIO (0x65)

The SIO interrupt-source-register contains all relevant information of the SIO-mode. All bits are set by hardware. An interrupt is generated if at least one of these bits is enabled via INT_EN_SIO and contains a ‘1’. Writing a ‘1’ to either of these bits clears this interrupt-source individually. Writing a ‘0’ to any of these bits has no effect.

Table 37: INT_SRC_SIO register

Bit	7	6	5	4	3	2	1	0
Name	Reserved					WURQ	CQ1_FALL	CQ1_RISE
Access	-					R/W1	R/W1	R/W1
Default	-					0	0	0

CQ1_RISE *Rising edge at Pin CQ1 (voltage changes from 0V to VS)*

CQ1_FALL *Falling edge at Pin CQ1 (voltage changes from VS to 0V)*

WURQ *Wakeup Request detected*

7.8.22. INT_EN_SIO (0x66)

The SIO interrupt-enable-register allows the user to enable each SIO interrupt-source individually.

Table 38: INT_EN_SIO register

Bit	7	6	5	4	3	2	1	0
Name	Reserved					WURQ_EN	CQ1_FALL_EN	CQ1_RISE_EN
Access	-					R/W	R/W	R/W
Default	-					0	0	0

CQ1_RISE_EN *Enables the interrupt source CQ1_RISE* *(0b: disabled 1b: enabled)*

CQ1_FALL_EN *Enables the interrupt source CQ1_FALL* *(0b: disabled 1b: enabled)*

WURQ_EN *Enables the interrupt source WURQ* *(0b: disabled 1b: enabled)*

7.8.23. INT_SRC_UART (0x67)

The UART interrupt-source-register contains all relevant information of the UART-mode. All bits are set by hardware. An interrupt is generated if at least one of these bits is enabled via INT_EN_UART and contains a ‘1’. Writing a ‘1’ to either of these bits clears this interrupt-source individually. Writing a ‘0’ to any of these bits has no effect.

Table 39: INT_SRC_UART register

Bit	7	6	5	4	3	2	1	0
Name	Reserved					RX_OVFLW	RX_REC	TX_RDY
Access	-					R/W1	R/W1	R/W1
Default	-					0	0	0

TX_RDY *UART is ready to send data. Data can be written to (0x24)*

RX_REC *UART received one octet. Received data can be fetched from (0x24)*

RX_OVFLW *UART receive overflow*

7.8.24. INT_EN_UART (0x68)

The UART interrupt-enable-register allows the user to enable each UART interrupt-source individually.

Table 40: INT_EN_UART register

Bit	7	6	5	4	3	2	1	0
Name	Reserved					RX_OVFLW_EN	RX_REC_EN	TX_RDY_EN
Access	-					R/W	R/W	R/W
Default	-					0	0	0

7.8.25. INT_SRC_FH (0x69)

The FH interrupt-source-register contains all relevant information of the frame handler mode. All bits are set by hardware. An interrupt is generated if at least one of these bits is enabled via INT_EN_FH and contains a ‘1’. Writing a ‘1’ to either of these bits clears this interrupt-source individually. Writing a ‘0’ to any of these bits has no effect.

Table 41: INT_SRC_FH register

Bit	7	6	5	4	3	2	1	0
Name	Reserved			TOUT	SOT	SOR	LVL	MSG
Access	-			R/W1	R/W1	R/W1	R/W1	R/W1
Default	-			0	0	0	0	0

MSG *End of Message (Triggers after the last character of a message was received)*

LVL *Message Level*

(Triggers if a defined amount of buffered characters is reached, see 7.8.15)

SOR *Start of Receiving (Triggers as soon as the device starts receiving a message)*

SOT *Start of Transmitting (Triggers when the device starts transmitting its message)*

TOUT *Timeout detected*

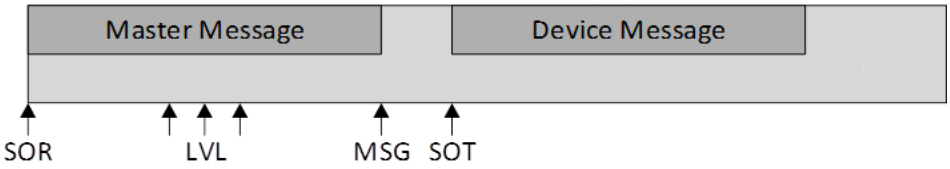


Figure 11: Interrupt Trigger Positions

7.8.26. INT_EN_FH (0x6A)

The FH interrupt-enable-register allows the user to enable each FH interrupt-source individually.

Table 42: INT_EN_FH register

Bit	7	6	5	4	3	2	1	0
Name	Reserved			TOUT_EN	SOT_EN	SOR_EN	LVL_EN	MSG_EN
Access	-			R/W	R/W	R/W	R/W	R/W
Default	-			0	0	0	0	0

MSG_EN *Enables the interrupt source MSG* *(0b: disabled 1b: enabled)*

LVL_EN *Enables the interrupt source LVL* *(0b: disabled 1b: enabled)*

SOR_EN *Enables the interrupt source SOR* *(0b: disabled 1b: enabled)*

SOT_EN *Enables the interrupt source SOT* *(0b: disabled 1b: enabled)*

TOUT_EN *Enables the interrupt source TOUT* *(0b: disabled 1b: enabled)*

7.8.27. CLK_OUT (0x6C)

This register controls the clock output of the chip. If the clock is not externally needed, the output pad for port CLK_EXT can be disabled via bit CLK_OUT_DIS.

Table 43: CLK_OUT register

Bit	7	6	5	4	3	2	1	0
Name	Reserved							CLK_OUT_DIS
Access	-							R/W
Default	-							1b

CLK_OUT_DIS Output Clock disable

0b CLK_EXT is not disabled

1b CLK_EXT is disabled

7.9. Interruption Handling

There are four interrupt source registers (7.8.19, 7.8.21, 7.8.23, 7.8.25) which can be individually enabled by configuring their corresponding interrupt enable registers. All enabled interrupt flags are logically “or”ed and the inverted result is connected to the pin INTX. By default, all interrupt sources are disabled at startup. There is no global interrupt enable.

The interrupt source bits are always set when a transition to the active state is observed at the related signals. This setting of bits is not disabled when the interrupt source is not enabled. To clear an interrupt the user (e. g. MCU) has to write a ‘1’ to the specific bit of the interrupt source register

7.10. SPI (Serial Peripheral Interface)

7.10.1. Signal Description

Table 44: Signal Description

Name	Type	Description
MOSI	Input	Data input
MISO	Output	Data output
SCLK	Input	Clock input (f_{MAX} = 20 MHz)
SSX	Input	Slave select (active-low)
INTX	Output	Interrupt output for microcontroller (active-low)

7.10.2. Data Format

The CCE4502 is configured as SPI slave and uses the CPOL=0, CPHA=0 configuration, i. e. SCLK is low in idle mode and the data has to be valid on the rising edge of SCLK. During each transaction, a minimum of 2 bytes have to be transferred. For bulk access to the frame-handler-buffer via the FHD register, n bytes can be transferred. The first received byte after a falling SSX edge always reflects the current status of the two channels. The format depends on the configured modes.

Figure 12 illustrates the timing of a SPI access and Table 45 contains the related timing characteristics.

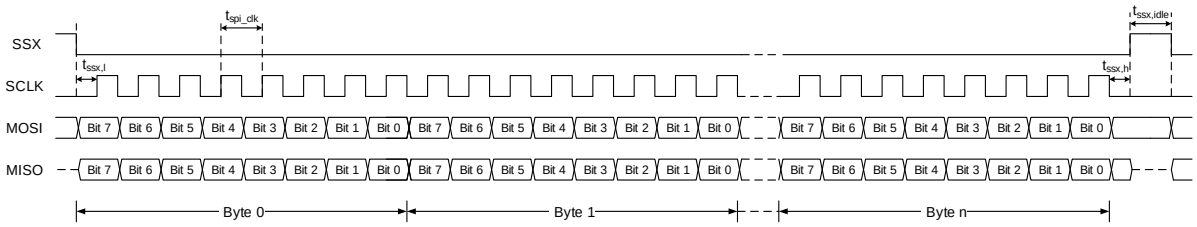


Figure 12: SPI timing diagram

Table 45: SPI timing characteristics

Characteristic	Symbol	Min.	Max.	Unit
SPI frequency	t_{spi_clk}		20	MHz
SSX high pulse	$t_{ssx,idle}$	70		ns
SSX low to SCLK high	$t_{ssx,l}$	35		ns
SCLK low to SSX high	$t_{ssx,h}$	35		ns

7.10.3. MOSI Format

Table 46: MOSI Format

Bit	7	6	5	4	3	2	1	0
1st Byte	ADR							R/W
2nd Byte	DATA							
	…							
nth Byte	DATA							

ADR **Address for register access**

0x20-0x3F	Channel 1 registers
0x40-0x5F	Channel 2 registers
0x60-0x7F	Common registers

R/W **Register access type**

b0	write to address
b1	read from address

DATA *Value for write access*

3rd – nth byte is optional; ignored on read access

7.10.4. MISO Format

Table 47: MISO Format

Bit	7	6	5	4	3	2	1	0
1st Byte	STAT							
2nd Byte	DATA							
	…							
nth Byte	DATA							

STAT **status of the IC (see 7.10.5)**

DATA **Current value on read access to register**
3rd – nth byte is optional; not valid on write access

7.10.5. STAT Format

Table 48: STAT Format

Mode	Mode Name	7	6	5	4	3	2	1	0
0b00	SIO Mode	HIGH_T	HIGH_VS	-	WURQ	SD2	SD1	MODE	
0b01	UART Mode	HIGH_T	RX_ERR	RX_RDY	TX_RDY	SD2	SD1	MODE	
0b10	IO-Link Mode	TOUT	FH_STAT			SD2	SD1	MODE	

MODE *IC mode*

0h: SIO Mode (default)
1h: UART Mode
2h: IO-Link Mode
3h: reserved

SD1/SD2 *Short Detection on CQ1 and DIO*

WURQ *Wake-Up on CQ1 detected, identical to INT_SRC_SIO.WURQ*

HIGH_VS *High voltage indicator*

HIGH_T *High temperature indicator*

TX_RDY *UART transmitter ready*

RX_RDY *UART receiver ready (input available)*

RX_ERR *UART parity error*

FH_STAT *Frame Handler state (see section 7.7.3)*

000b: IDLE
001b: Transmission inactive; frame handler waits for data at register FHD
010b: Transmission active; no further data required
011b: Transmission active; frame handler waits for data at register FHD
100b: Receiving active
101b: Receiving active; new input available, read register FHD
110b: Receiving active; received message is erroneous
111b: Receiving active; received message is erroneous; new input available

TOUT *Frame handler timeout (see section 7.7.3)*

0b: No timeout detected
1b: Timeout detected

8. Application Notes

8.1. Power Dissipation Constraints

The CCE4502 QFN24 package has a thermal resistance of 40 K/W from silicon junction to ambient using an optimized PCB design. With maximum ambient temperature of 105 °C and maximum junction temperature of 150 °C a maximum power dissipation of 1.125 W can be handled by the thermal capabilities of the QFN package.

Following table gives an exemplary overview of the power contributions of the different circuit blocks contained in the CCE4502 and calculated at nominal condition V(L+) = 24 V and VHH = 7 V.

Table 49: CCE4502 Power contributions

Circuit Block	Voltage Drop	Current	Power
IO Channel 1	2 V	200 mA	0.400 W
IO Channel 2	2 V	200 mA	0.400 W
5/3.3V Regulator (at 3.3V), Reference	3.7 V	50 mA	0.185 W
5V Regulator	19 V	10 mA	0.190 W
1.8V Regulator (internal)	5.2 V	3 mA	0.016 W
DC/DC Converter (in buck mode)	17 V	60 mA	0.204 W
DC/DC Converter (in linear mode)	17 V	60 mA	1.020 W

The calculated power sum with nearly 1.4 Watt (DC/DC in buck mode) shows that tradeoffs must be made in the overall system design and by using the different features of the CCE4502 IC.

8.2. Application with DC / DC Converter in Buck Mode

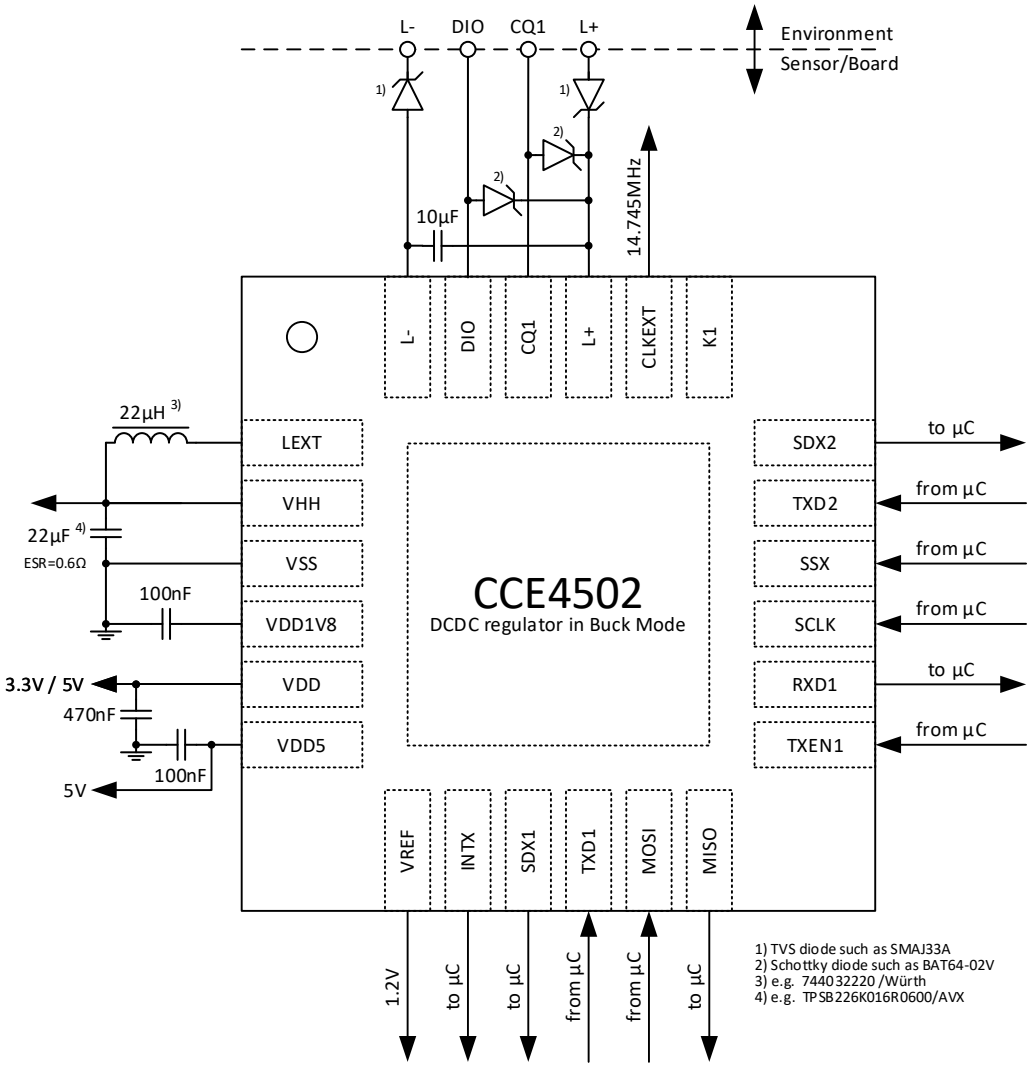


Figure 13: Application with active DC/DC Converter (Supply Mode 1)

8.3. Application with DC / DC Converter in Linear Mode

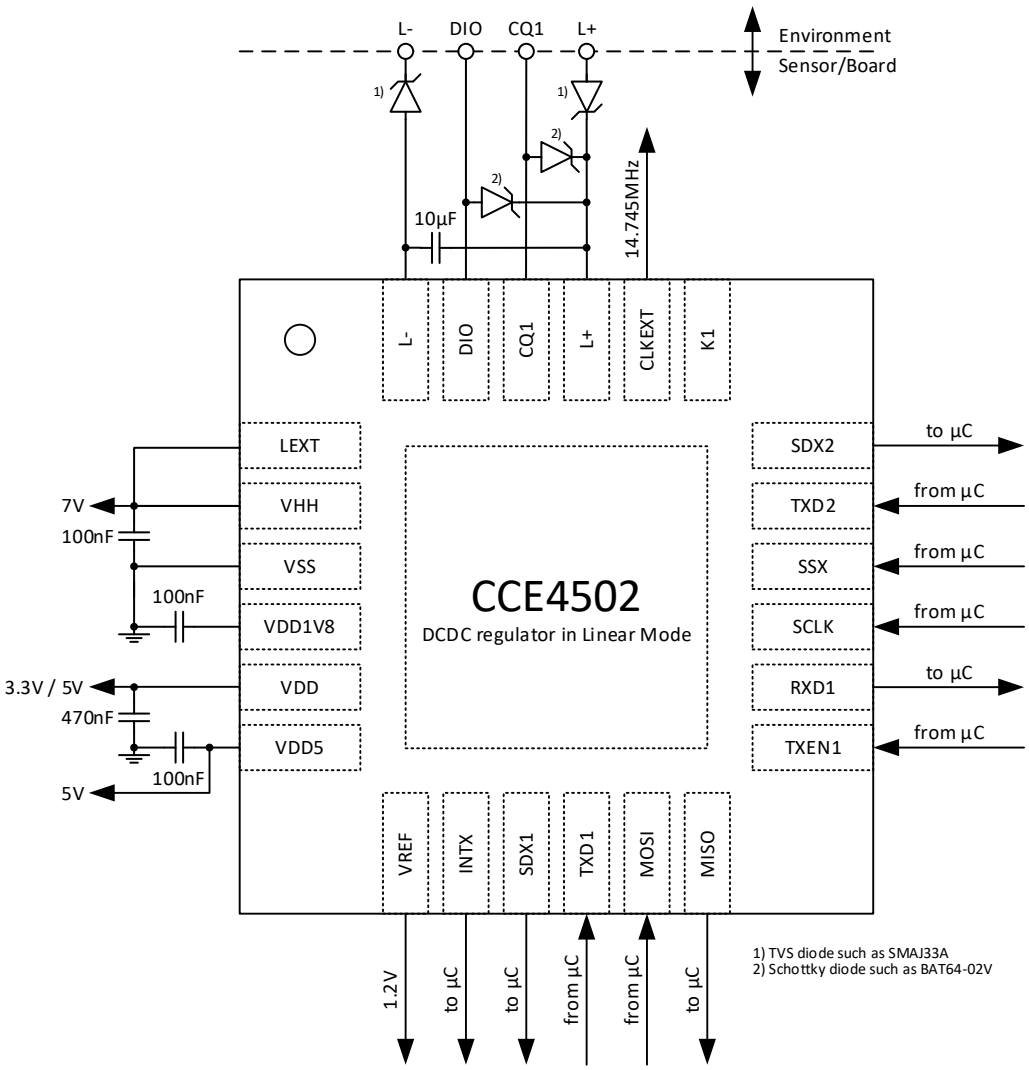


Figure 14: Application with disabled DC/DC Converter (Supply Mode 2)

8.4. Application with External Supply

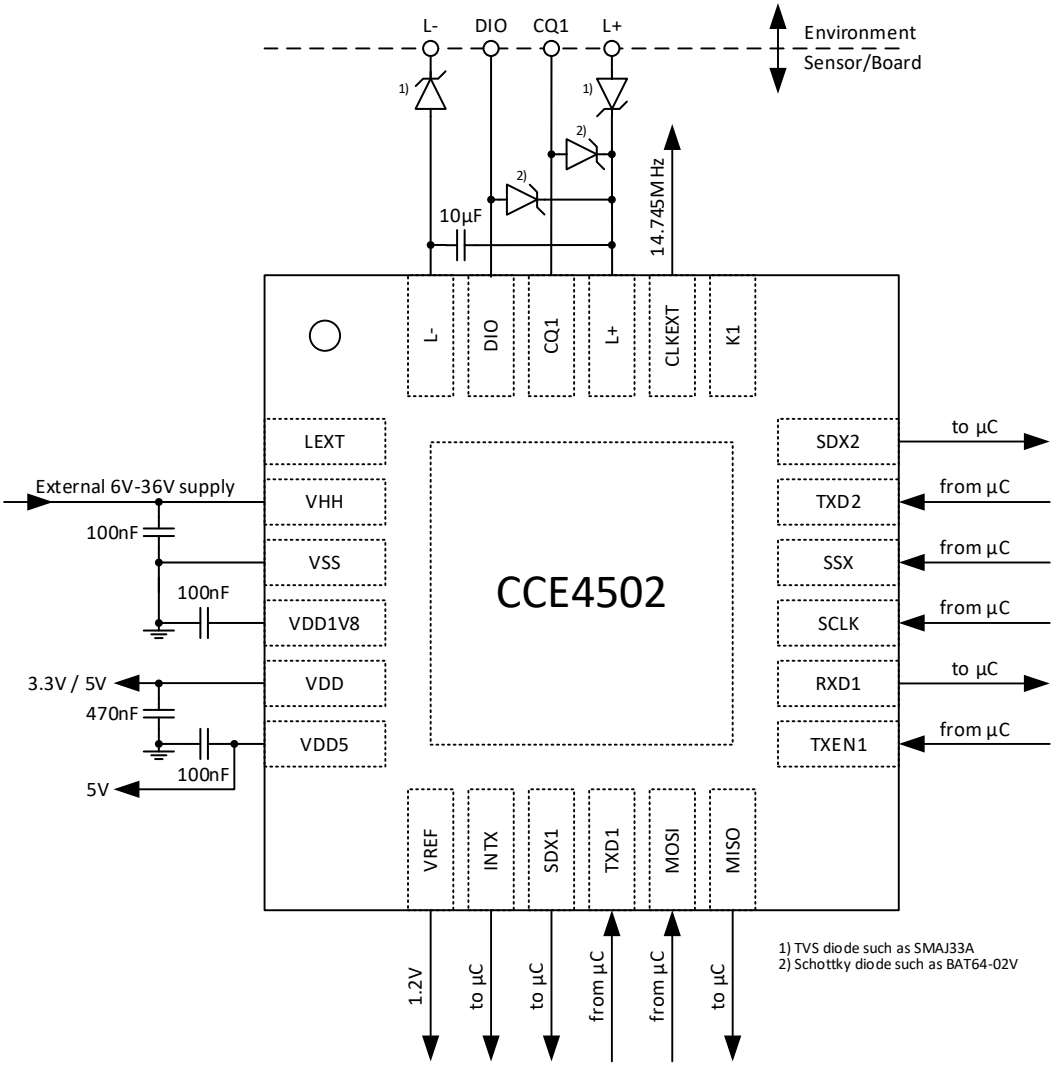


Figure 15: Application with external supply (Supply Mode 3)

9. Package Outline

9.1. QFN24 Package

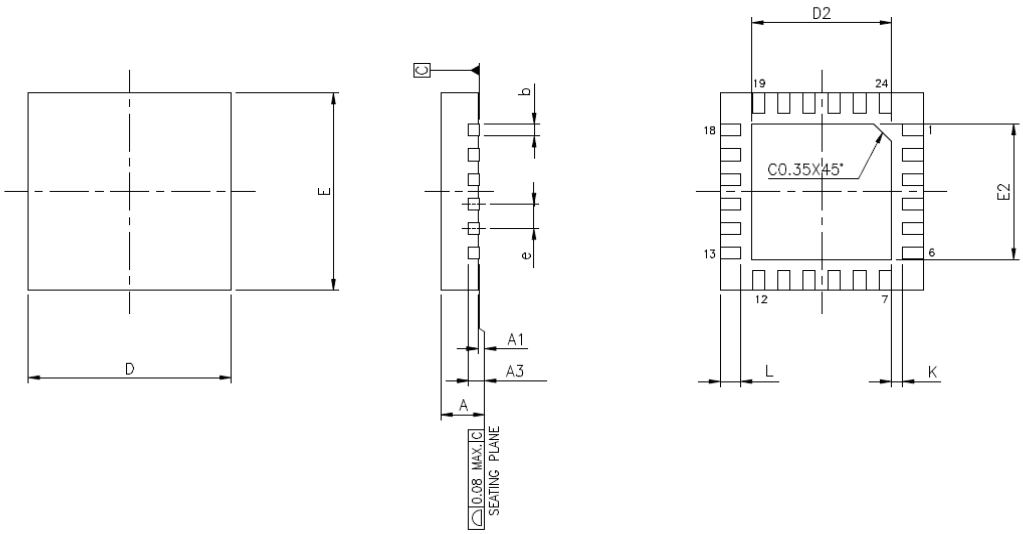


Figure 16: QFN24 Package. Drawing not to scale!

Symbol	A	A1	A3	b	D	E	e	L	K	D2	E2
Min	0.70	0.00	0.20 REF.	0.18	4.00 BSC.	4.00 BSC.	0.50 BSC.	0.35	0.20	2.50	2.50
Typ	0.75	0.02		0.25				0.40	-	2.60	2.60
Max	0.80	0.05		0.30				0.45	-	2.65	2.65

UNIT: mm

NOTES :
1. JEDEC OUTLINE : MO-220 WGGD-6.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. THE MINIMUM "K" VALUE OF 0.20mm APPLIES.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

9.2. Chip Scale Package (Bumped Die)

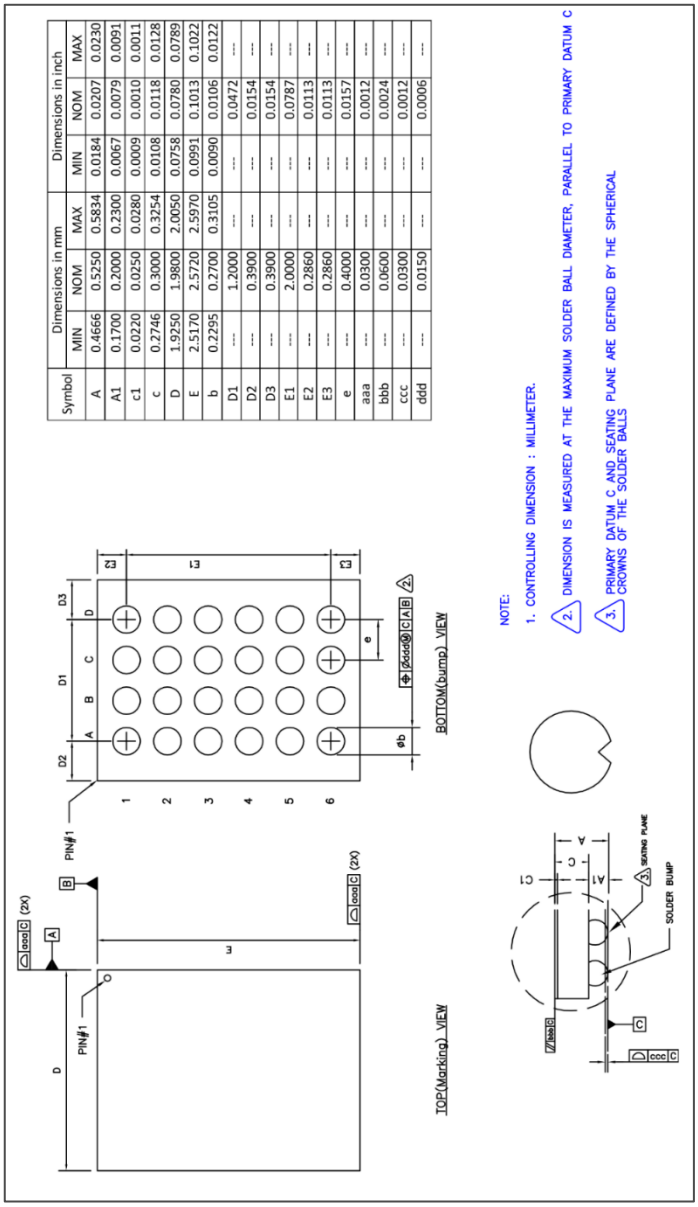
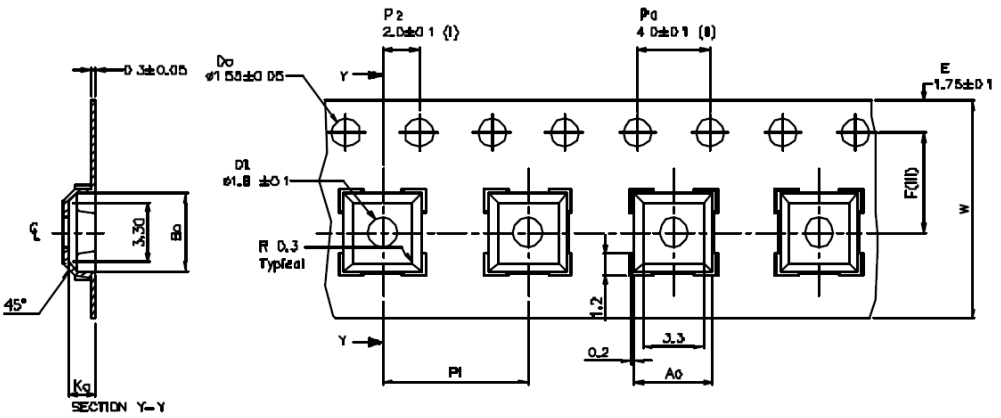


Figure 17: CSP package drawing

10. Tape and Reel Information

10.1. Tape QFN24 Package

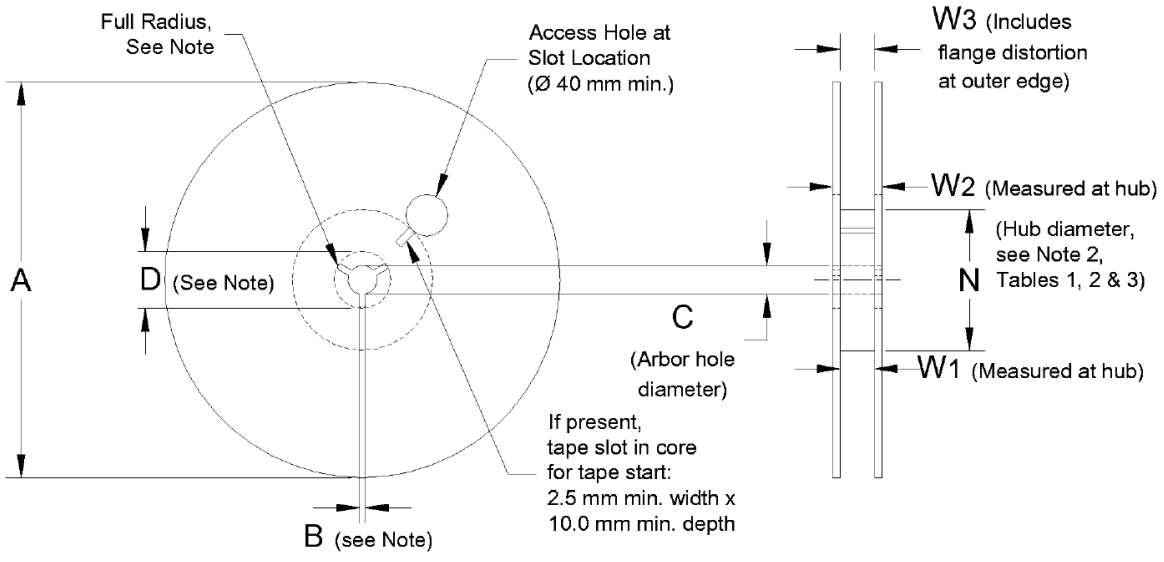


A0	4.30 +/– 0.1
B0	4.30 +/– 0.1
K0	1.50 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

10.2. Reel Information



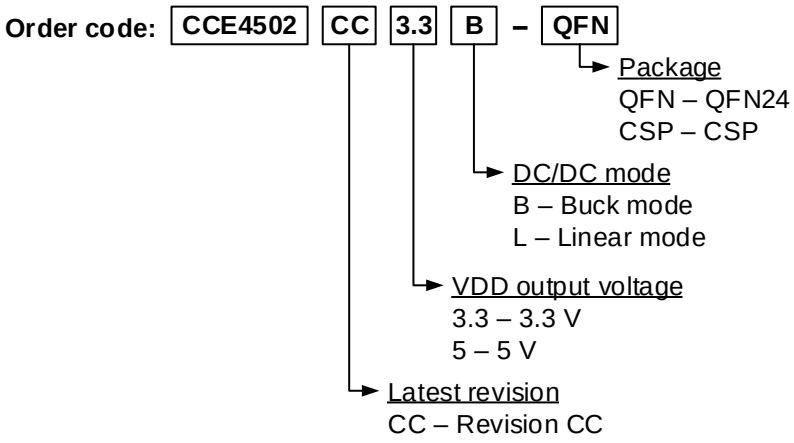
Note: Drive spokes optional; if used, dimensions B and D shall apply.

Figure 18: Reel Dimensions

Symbol	A	B	C	D	W_1 QFN24
Min	-	1.5	12.8	20.2	13.25
Typ	-	-	13.0	-	-
Max	330	-	13.5	-	13.75

11. Ordering Information

Parts are available as in QFN or CSP package, delivered in tape&reel or tray, with buck mode or linear mode DC/DC converter function and 3.3V or 5V VDD output voltage. Please find your order code below and visit dialog-semiconductor.com/contact/inquiry for an individual quote.



12. Revision History

Revision	Date	Description
2.6	8-Mar-2023	4.1: Updated Chip Scale Package Drawing 4.2: Added missing pull down to CLK_EXT description 5, 6: Indexed parameters and improved parameter names Document layout changes 7.8: Added Bit “TEST_FACTORY_RESET” to register STAT @addr 0x62 7.8: Added 2 Bits (“CONF_FDEL) to register FHC @addr 0x25 8: Updated Application Drawings (protection circuitry) Updated Legal Disclaimer
2.5	17-Feb-2022	Rebranding
2.4	31-Jul-2020	Pinout: added exp. pad to VSS, corrected type/domain of VDD5 Parameters: Added condition to Fclk Parameters: Corrected invalid VL+ range in condition of VDD5 line reg Recommendation to use linear mode devices for supply mode 3 Update ordering information Corrected cosmetic errors
2.3	03-Jun-2020	Updated REV to 0x40 Corrected format errors
2.2	05-May-2020	Recommending 10 µF between L+ and L- for all supply modes
2.1	08-Apr-2020	Revised absolute max. ratings, electrical characteristics Revised reverse polarity protection Corrected power supply schematic and VDD5 description (7.3) Updated Template
2.0	20-Jan-2020	Revised CSP marking Revised absolute max. ratings, electrical characteristics Revised reverse polarity protection Revised application notes (DC/DC buck mode: schottky diode is no longer required)
1.4	31-Oct-2019	Updated Template
1.3	03-Jul-2018	Minor Corrections in Register and Interrupt Description
1.2	06-June-2018	Revised Power Dissipation Example Revised Reverse Polarity Protection
1.1	18-Apr-2018	Updated CSP Package Drawing Added C, L, D Examples in Application Circuit Buck Mode Revised Frame Handler Section, FHC (0x25), STAT (0x62) and SPI STAT byte
1.0	18-Jan-2018	Initial version.